S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Christopher K. Morzano	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.024US4
Title:	HIGH SPEED PROGRAMMABLE COUNTER	

PRELIMINARY AMENDMENT

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

Before taking up the above-identified application for examination, please enter the following amendments.

IN THE SPECIFICATION

After the title, please insert the following paragraph:

This application is a Divisional of U.S. Application No. 09/314,061, filed May 18, 1999, which is a Divisional of U.S. Application No. 08/900,734, filed July 25, 1997, now U.S. Patent No. 5,907,591, which is a Continuation of U.S. Application No. 08/535,655, filed September 28, 1995, now U.S. Patent No. 5,666,390.

IN THE CLAIMS

Please cancel claims 1-9 and add the following the new claims:

10. (New) A switch comprising:

a plurality of serial input ports coupled to a first bus;

a memory coupled to the input ports; and

a plurality of serial output ports coupled to the memory and to a second bus, wherein each serial input port and each serial output port are coupled to a programmable counter having programmable start and stop values.

11. (New) The switch of claim 10, and further comprising:

a parity generator coupled between the serial input ports and the memory; and

a parity checker coupled between the memory and the serial output ports.

12. (New) The switch of claim 10 wherein each of the serial input and serial output ports are double buffered.

13. (New) The switch of claim 10 and further comprising:

a controller coupled to the switch for controlling routing of ATM cells of data between the serial input ports and the serial output ports.

14. (New) An ATM switch comprising:

a plurality of serial input ports coupled to a first bus;

a memory coupled to the input ports; and

a plurality of serial output ports coupled to the memory and to a second bus, wherein each serial input port and each serial output port are coupled to a programmable counter comprising:

multiple latches for providing a count output;

a start count circuit coupled to the latches;

a stop count circuit coupled to said latches;

a maximum count circuit coupled to the latches; and

a compare circuit coupled to the stop count circuit and the latches.

15. (New) The ATM switch of claim 14 and further comprising a controller coupled to the switch for controlling routing of ATM cells of data between serial input ports and serial output ports.

16. (New) The ATM switch of claim 14, and further comprising:

a parity generator coupled between the serial input ports and the memory; and

a parity checker coupled between the memory and the serial output ports.

17. (New) The ATM switch of claim 14, wherein each of the serial input ports and the serial output ports are double buffered.

Claims 10-17 are now pending in this application. Applicant will file additional claims in a Supplemental Preliminary Amendment. The Examiner is invited to contact the below-signed attorney if examination begins prior to receiving the additional claims.

Respectfully submitted,

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